UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,602	08/30/2001	Scott Van De Graaff	M4065.0469/P469	6439

24998 7590 12/19/2002

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER
AUDUONG, GENE NGHIA

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,602	VAN DE GRAAFF, SCOTT	
	Examiner	Art Unit	
	Gene N Auduong	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-55 is/are pending in the application.

4a) Of the above claim(s) 29-55 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12,14-26 and 28 is/are rejected.

7)☒ Claim(s) 13 and 27 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Response of Election/Restrictions

1. It's noted that this application was originally examining by Examiner Kennedy, Jennifer, in a different class (class 438) prior the restriction/election. Applicants' attorney response to the election/restriction and elected Group I, claims 1-28 and now being examining in class 365.

Claims 29-55 are canceled and withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention in Paper No. 5.

Drawings

2. The corrected or substitute drawings were received on October 11, 2001. These drawings are acceptable.

Information Disclosure Statement

3. The office acknowledges receipt of information disclosure statement filed December 4, 2001. The information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4, 6-12, 15-19 and 21-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Ingalls (U.S. Pat. No. 5,892,716).

Regarding claim 1, Ingalls discloses a programmable circuit 110 for a plurality of programmable elements 112, the programming circuit (see figure 5) comprising: a plurality of

programmable elements (programmable anti-fuse elements 112); a plurality of element programming circuits (programmable anti-fuse circuit 110) each associated with a programmable element 112 and each including a latch circuit (latch circuit 120; its detail circuit is showing in figure 4a) for receiving and holding a desired programming state of an associated programmable element (state of an anti-fuse programmable element 112), the plurality of element programming circuits 110 setting the state of the associated programmable elements 112 in accordance with a desired programming state held in an associated latch (latch circuit 120) in response to a common control signal CGND (col. 8, lines 20–27; col. 4, line 45 – col. 6, line 53, col. 2, lines 6-22).

Regarding claim 2, Ingalls discloses a circuit as in claim 1, wherein each of the latch circuit 120 (see figures 4a) comprises: an inverter circuit (inverter 140) having an input coupled to an input (input node 138) of the latch circuit 120 and an output coupled to an output of the latch circuit 120 (output signal node of latch circuit 120); a pair of n-channel transistors (n-channel transistors 144, 146) connected in series between an input 138 of the latch circuit 120 and a first reference voltage (ground voltage connected to transistor 146); a pair of p-channel transistors (p-channel transistors 132, 134) connected in parallel between the input 138 of the latch circuit 120 and a second reference Vcc; a read-and-latch signal line (control signal RDFUS*) coupled to control gates of a first of the pair of p-channel transistors (gate of transistor 132) and a first of the pair of n-channel transistors (gate of transistor 144); wherein the output of the inverter circuit 140 is coupled to control gates of a second of the pair of p-channel transistors (gate of transistor 134) and a second of the pair of n-channel transistors (gate of transistor 146).

Regarding claim 3, Ingalls discloses a circuit as in claim 2, wherein the read-and-latch signal line is configured to apply a read-and-latch signal (RDFUS* signal) to permit reading and latching of the desired programming signal (col. 4, line 45 – col. 5, line 5).

Regarding claim 4, Ingalls discloses a circuit as in claim 2, wherein a third p-channel transistor (p-channel transistors 124 or 128) is coupled between the pair of parallel-connected p-channel transistors 132, 134 and the second reference voltage Vcc, the third p-channel transistor (transistor 124 or 128) having a gate coupled to the first reference voltage (transistor 124 or 128 having control gate coupled to ground voltage).

Regarding claim 6, Ingalls discloses a circuit as in claim 1, wherein the common control signal CGND includes a voltage sufficient to change a state of the associated programmable elements 112 (col. 2, lines 6 – 22).

Regarding claim 7, Ingalls discloses a programming circuit for a programmable element (see figure 5), comprising: at least one latch circuit (latch circuit 120; its detail circuit is showing in figure 4a); at least one latch-programming circuit 110 for temporarily applying a programming signal to an input of a respective latch circuit 120, the latch circuit 120 latching a state of the programming signal (figure 4a, output latch portion 123 for receiving its control signal RDFUS* at control gate of transistor 144 and programming signal output from the anti-fuse sensing portion 125 to input node 138 to control the latching state of programmed signal from programmable anti-fuse 112, col. 6, lines 22–34); a signal line applying a voltage (signal CGND) sufficient to change the state of the programmable element 112 (also see figure 4a and 2a, switchable signal CGND applying a high voltage sufficient enough to cause the anti-fuse 112 to breakdown/blow, col. 2, lines 15 – 18); at least one latch isolation transistor (transistor 152)

coupled between the programmable element 112 and the latch circuit 120; at least one state control transistor 146 coupled between the programmable element 112 and a first reference voltage (ground voltage) and having a gate controlled by an output of the latch circuit 120 (figure 4a, control gate of transistor 146 controls by output signal of output latch 123); wherein during a programming phase, the latch circuit 120 is configured to latch the programming signal, and during a common control phase, the latch isolation transistor 152 is configured to decouple the programmable element 112 from the latch circuit 120 and the signal line (signal CGND) is configured to apply the state-changing voltage to the programmable element 112 if the output of the latch circuit 120 turns on the state control transistor 146 (col. 8, lines 20–27; col. 4, line 45 – col. 6, line 53, col. 2, lines 6-22).

Regarding claim 8, Ingalls discloses a circuit as in claim 7, wherein the at least one latch circuit 120 (see figure 4a) comprises: an inverter circuit 140 having an input coupled to the input 138 of the latch circuit 120 and an output coupled to the output of the latch circuit (output signal node); a pair of n-channel transistors 144, 146 connected in series between an input of the latch circuit 120 and the first reference voltage (ground voltage); a pair of p-channel transistors 132, 134 connected in parallel between the input 138 of the latch circuit 120 and a second reference voltage Vcc; a read-and-latch signal line (control signal RDFUS*) coupled to control gates of a first of the pair of p-channel transistors (gate of transistor 132) and a first of the pair of n-channel transistors (gate of transistor 144); wherein the output of the inverter circuit 140 is coupled to control gates of a second of the pair of p-channel transistors (gate of transistor 134) and a second of the pair of n-channel transistors (gate of transistor 146).

Regarding claim 9, Ingalls discloses a circuit as in claim 8, wherein the read-and-latch signal line is configured to apply a read-and-latch signal (signal RDFUS*) during the programming phase to permit reading and latching of the programming signal (figures 4a, col. 4, line 45 – col. 5, line 5).

Regarding claim 10, Ingalls discloses a circuit as in claim 8, wherein a third p-channel transistor (p-channel transistors 124 or 128) is coupled between the pair of parallel connected p-channel transistors 132, 134 and the second reference voltage Vcc, the third p-channel transistor (transistor 124 or 128) having a gate coupled to the first reference voltage (ground voltage).

Regarding claim 11, Ingalls discloses a circuit as in claim 7, further comprising at least one programming enable transistor 144 configured to couple the state control transistor 146 to the programmable element 112 during the common control phase (col. 4, line 45 – col. 6, line 53).

Regarding claim 12, Ingalls discloses a circuit as in claim 7, further comprising at least one programmable element isolation transistor 150 configured to decouple the programmable element 112 from the latch circuit 120 and the latch-programming circuit during the programming phase (col. 4, line 45 – col. 6, line 53).

Regarding claim 15, Ingalls discloses a circuit as in claim 7, wherein the state-changing voltage (signal CGND) includes a voltage sufficient to blow an anti-fuse 112 (col. 2, lines 6 – 22).

Regarding claim 16, Ingalls discloses a memory circuit (figure 6, memory circuit 10), comprising: a plurality of memory elements (figure 1, array of memory cells 14); and at least one

programming circuit (see figure 5, programmable anti-fuse circuit 110) associated with a plurality of programmable elements 112 (see figure 5, programmable element 112) and configured to activate one or more of the plurality of memory elements 112, the programming circuit 110 comprising: a plurality of programmable elements 112; a plurality of element programming circuits 110 each associated with a programmable element 112 and each including a latch circuit 120 for receiving and holding a desired programming state of an associated programmable element 112, the plurality of element programming circuits 110 setting the state of the associated programmable elements 112 in accordance with a desired programming state held in an associated latch 120 in response to a common control signal CGND (col. 8, lines 20–27; line 37-43, col. 4, line 45 – col. 6, line 53, col. 2, lines 6-22).

Regarding claim 17, Ingalls discloses a memory circuit as in claim 16, wherein each of the latch circuit 120 (see figure 4a) comprises: an inverter circuit 140 having an input coupled to an input 138 of the latch circuit 120 and an output coupled to an output of the latch circuit 120 (output node of latch circuit 120); a pair of n-channel transistors 144, 146 connected in series between an input 138 of the latch circuit 120 and a first reference voltage (ground voltage); a pair of p-channel transistors 132, 134 connected in parallel between the input 138 of the latch circuit 120 and a second reference voltage Vcc; a read-and-latch signal line (control signal RDFUS*) coupled to control gates of a first of the pair of p-channel transistors (control gate of transistor 132) and a first of the pair of n-channel transistors (control gate of transistor 144); wherein the output of the inverter circuit 140 is coupled to control gates of a second of the pair of p-channel transistors (control gate of transistor 134) and a second of the pair of n-channel transistors (control gate of transistor 146).

Regarding claim 18, Ingalls discloses a memory circuit as in claim 17, wherein the read-and-latch signal line is configured to apply a read-and-latch signal (control signal RDFUS*) to permit reading and latching of the desired programming signal (col. 4, line 45 – col. 5, line 5).

Regarding claim 19, Ingalls discloses a memory circuit as in claim 17, wherein a third p-channel transistor (transistor 124 or 128) is coupled between the pair of parallel connected p--channel transistors 132, 134 and the second reference voltage Vcc, the third p-channel transistor having a gate coupled to the first reference voltage (transistor 124 or 128 having control gate coupled to ground voltage).

Regarding claim 21, Ingalls discloses a memory circuit (figure 6, memory circuit 10), comprising: a plurality of memory elements (figure 1, array of memory cells 14); and at least one programming circuit (see figure 5, programmable anti-fuse circuit 110) associated with a plurality of programmable elements 112 (see figure 5, programmable element 112) and configured to activate one or more of the plurality of memory elements 112, the programming circuit 110 comprising: at least one latch circuit 120 (its detail circuit is showing in figure 4a); at least one latch-programming circuit 110 for temporarily applying a programming signal to an input of a respective latch circuit 120, the latch circuit latching a state of the programming signal (figure 4a, output latch portion 123 for receiving its control signal RDFUS* at control gate of transistor 144 and programming signal output from the anti-fuse sensing portion 125 to input node 138 to control the latching state of programmed signal from programmable anti-fuse 112, col. 6, lines 22–34); a signal line (signal CGND) applying a voltage sufficient to change the state of the programmable element (also see figure 4a and 2a, switchable signal CGND applying a high voltage sufficient enough to cause the anti-fuse 112 to breakdown/blow, col. 2, lines 15 –

18); at least one latch isolation transistor (transistor 152) coupled between the programmable clement 112 and the latch circuit 120; at least one state control transistor 146 coupled between the programmable element 112 and a first reference voltage (ground voltage) and having a gate controlled by an output of the latch circuit 120 (control gate of transistor 146 controls by output signal of the output latch 123); wherein during a programming phase, the latch circuit 120 is configured to latch the programming signal, and during a common control phase, the latch isolation transistor 152 is configured to decouple the programmable element 112 from the latch circuit 120 and the signal line is configured to apply the state-changing voltage (signal CGND) to the programmable element 112 if the output of the latch circuit turns on the state control transistor 146 (col. 8, lines 20–27; lines 37-43, col. 4, line 45 – col. 6, line 53, col. 2, lines 6-22).

Regarding claim 22, Ingalls discloses a memory circuit as in claim 21, wherein the at least one latch circuit 120 (its detail circuit is showing in figure 4a) comprises: an inverter circuit 140 having an input coupled to the input 138 of the latch circuit 120 and an output coupled to the output of the latch circuit (output of inverter 140 coupled to the output of output latch 123); a pair of n-channel transistors 144, 146 connected in series between an input 138 of the latch circuit 120 and the first reference voltage (ground voltage); a pair of p-channel transistors 132, 134 connected in parallel between the input 138 of the latch circuit 120 and a second reference voltage Vcc; a read-and-latch signal line (control signal RDFUS*) coupled to control gates of a first of the pair of p-channel transistors (control gate of transistor 132) and a first of the pair of n-channel transistors (control gate of transistor 144); wherein the output of the inverter circuit 140 is coupled to control gates of a second of the pair of p-channel transistors (control gate of transistor 134) and a second of the pair of n-channel transistors (control gate of transistor 146).

Regarding claim 23, Ingalls discloses a memory circuit as in claim 22, wherein the read-and-latch signal line is configured to apply a read-and-latch signal (control signal RDFUS*) during the programming phase to permit reading and latching of the programming signal (figures 4a, col. 4, line 45 – col. 5, line 5).

Regarding claim 24, Ingalls discloses a memory circuit as in claim 22, wherein a third p--channel transistor (transistor 124 or 128) is coupled between the pair of parallel-connected p-channel transistors 132, 134 and the second reference voltage Vcc, the third p-channel transistor having a gate coupled to the first reference voltage (transistor 124 or 128 having control gate coupled to ground voltage).

Regarding claim 25, Ingalls discloses a memory circuit as in claim 21, further comprising at least one programming enable transistor 144 configured to couple the state control transistor 146 to the programmable element 112 during the common control phase (col. 4, line 45 – col. 6, line 53).

Regarding claim 26, Ingalls discloses a memory circuit as in claim 21, further comprising at least one programmable element isolation transistor 150 configured to decouple the programmable element 112 from the latch circuit 120 and the latch programming circuit 110 during the programming phase (col. 4, line 45 – col. 6, line 53).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5, 14, 20 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ingalls (U.S. pat. No. 5,892,716).

Regarding claim 5, Ingalls discloses a programmable circuit comprising all of the limitation as previously discussed in as in claim 1. Ingalls does not specifically disclose wherein the common control signal (control signal CGND) includes a voltage of between approximately 8 and 9 volts.

However, Ingalls disclose the control signal CGND includes a voltage sufficient to change a state of the associated programmable elements 112, and this voltage is large enough to ensure the break-down the anti-fuse 112 but not greater the maximum allowable impedance and this value is being calculated base on the value and size of components being used in the circuit (col. 2, lines 6 – 22, col. 5, lines 44-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ingalls's circuit to further disclose an approximate voltage range for the common control signal CGND of between approximately 8 and 9 volts or any other voltage range within the maximum allowable range without damage the device and best working condition for the device as design choice.

Regarding claim 14, Ingalls discloses a programmable circuit comprising all of the limitation as previously discussed in as claim 7. Ingalls does not specifically disclose wherein during the common control phase, the state-changing voltage (control signal CGND) of between approximately 8 and 9 volts is applied to the signal line.

However, Ingalls disclose the control signal CGND includes a voltage sufficient to change a state of the associated programmable elements 112, and this voltage is large enough to ensure the break-down the anti-fuse 112 but not greater the maximum allowable impedance and

this value is being calculated base on the value and size of components being used in the circuit (col. 2, lines 6 – 22, col. 5, lines 44-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ingalls's circuit to further disclose wherein during the common control phase, the state-changing voltage of between approximately 8 and 9 volts is applied to the signal line or any other voltage range within the maximum allowable range without damage the device and best working condition for the device as design choice.

Regarding claim 20, Ingalls discloses a programmable circuit comprising all of the limitation as previously discussed in as in claim 16. Ingalls does not specifically disclose wherein the common control signal (control signal CGND) includes a voltage of between approximately 8 and 9 volts.

However, Ingalls disclose the control signal CGND includes a voltage sufficient to change a state of the associated programmable elements 112, and this voltage is large enough to ensure the break-down the anti-fuse 112 but not greater the maximum allowable impedance and this value is being calculate based on the value and size of components being used in the circuit (col. 2, lines 6 – 22, col. 5, lines 44-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ingalls's device to further disclose an approximate voltage range for the common control signal CGND of between approximately 8 and 9 volts or any other voltage range within the maximum allowable range without damage the device and best working condition for the device as design choice.

Regarding claim 28, Ingalls discloses a programmable circuit comprising all of the limitation as previously discussed in as in claim 21, wherein during the common control phase,

the state-changing voltage (control signal CGND) of between approximately 8 and 9 volts is applied to the signal line.

However, Ingalls disclose the control signal CGND includes a voltage sufficient to change a state of the associated programmable elements 112, and this voltage is large enough to ensure the break-down the anti-fuse 112 but not greater the maximum allowable impedance and this value is being calculate based on the value and size of components being used in the circuit (col. 2, lines 6 – 22, col. 5, lines 44-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ingalls's circuit to further disclose wherein during the common control phase, the state-changing voltage of between approximately 8 and 9 volts is applied to the signal line or any other voltage range within the maximum allowable range without damage the device and best working condition for the device as design choice.

Allowable Subject Matter

8. Claims 13 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not show or suggest, in addition to other element in the claim, claiming the specific structure arrangement as claimed in claims 13 and 27. The latch programming circuit as claimed in claims 7 and 21, wherein the latch-programming circuit comprises at least one latch-programming transistor having a gate controlled by a first latch-programming signal, a first source/drain coupled to a second latch-programming signal,

and a second source/drain coupled to the input of the latch circuit through the latch isolation transistor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (703) 305-1343.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

GA
December 4, 2002

Gene N Auduong
Examiner
Art Unit 2818